AMENDMENTS TO THE SPECIFICATION

Page 14, 2nd full paragraph:

With the aforesaid arrangement of the semiconductor device, the n+-type emitter region 20 is electrically connected to the p^+-type substrate 10 through the intermediary of the second polycrystalline silicon layer 36, the barrier metal layer 46, the emitter electrode [[C]] E, the third conducting path P3, the sub-emitter electrode SE, and the p^+-type sub-emitter region 26. The p^+-type substrate 10 is electrically connected to the island 52 of the lead frame through the intermediary of the metallized layer 50, and is grounded when being used. Namely, the electrical connection of the emitter electrode E to the p^+-type substrate 10 is established in an interior of the semiconductor device without using any bonding-wire, for the grounding of the n^+-type emitter region 20.

Page 15, 3rd full paragraph:

As is apparent from Figs. 1 and 2, in the first embodiment of the semiconductor device according to the present invention, the p^+-type sub-emitter region 26 is widely extended so as to encompass the base-bonding pad [[CP]] BP, and is electrically connected to the p^+-type substrate 10 through the intermediary of the p^+-type diffusion buried region 24. Thus, although thermal noises are generated in the high resistance n^--type epitaxial layer 12 and p^--type epitaxial layer 16, and although a parasitic capacitance is produced due to the first, second, and fourth insulation layers 28, 38, and 40 which serve as a dielectric under the base-bonding pad BP, these thermal noises are prevented from being input to the base-bonding pad [[CP]] BP, because the thermal

noises can escape to the ground through the p^+-type sub-emitter layer 26 and the p^+-type diffusion buried region 24, whereby a noise factor (NF) characteristic can be considerably improved.

Pages 22-23, bridging paragraph:

In the second embodiment, when a part of the first polycrystalline silicon layer 30 is left on the first insulation layer 28 as shown in Fig. 23, another part 30a of the first polycrystalline silicon layer 30 is left on the first insulation layer [[30]] 28 as a conductive layer so as to cover the p^+-type sub-emitter region 26, as shown in Fig. 25, and thus the base-bonding pad BP is encompassed with the left part or conductive layer 30a of the first polycrystalline silicon layer 30.

Page 23, 3rd full paragraph:

In this first modification (shown in Fig. 26), an extent of the p^+-type sub-emitter region 26 is restricted so that only a part of the base-bonding pad BP is encompassed with the p^+-type sub-emitter region 26. ~~Namely~~, In contrast, the base-bonding pad BP is shown completely encompassed with the p^+-type sub-emitter region 26[[,]] in Fig. 25. Nevertheless, it is possible to effectively and securely prevent the inputting of the thermal noise from the epitaxial layers 12 and 16 into the base-bonding pad BP, because the base-bonding pad BP is completely encompassed with a conductive layer 30a of the first polycrystalline silicon layer 30.

Pages 24-25, bridging paragraph:

In this third embodiment, a p^+-type channel stopper region 26a is formed in the n^--type epitaxial layer 16 to cover the p^+-type diffusion buried layer 24, and a field silicon dioxide layer 78 is then formed on the p^+-type channel, using a Local Oxidation of Silicon (LOCOS) method. Then, a first insulation layer 28 and a first polycrystalline silicon layer 30 are formed and laminated in order on the n^--type epitaxial layer 16 having the field silicon dioxide layer 78, and are processed in substantially the same manner as in the above-mentioned first embodiment. Subsequently, a second insulation layer 32 and a second polycrystalline silicon layer 36 are formed and laminated in order on the first polycrystalline silicon layer, and are processed in substantially the same manner as in the above-mentioned first embodiment. Thereafter, third and fourth insulation layers 38 and 40 are formed as shown in Fig. [[26]] 24.